Amendments to the Abstract:

Please replace the Abstract, on page 25 of the specification as originally file, with the following:

A ~~processor element~~ data processing unit, structured to execute a 32-bit fixed length instruction set architecture, is backward compatible with a 16-bit fixed length instruction set architecture. ~~by translating each~~ Each of the 16-bit instructions received by the unit are translated into ~~a sequence of one or more~~ 32-bit instructions, with some 16-bit instructions requiring a sequence of multiple 32-bit instructions. A set of 32-bit instructions includes additional 32-bit instructions, not necessary for normal 32-bit operation, allowing the 32-bit instructions to emulate 16-bit instructions. This emulation allows the 32-bit instruction set to produce results corresponding to both 16-bit operations and 32-bit operations. Switching between 16-bit instruction execution and 32-bit instruction execution is accomplished in one embodiment by branch instructions that employ a least significant bit position of the address of the target of the branch to identify whether the target instruction is a 16-bit instruction or a 32-bit instruction.